[0043] Output pin CO controls the conductivity of transistor **211** with pins C1 to C5 having similar conductivity control upon transistors **213**, **214**, **212**, **215** and **216** respectively.

[0044] Transistors **211** and **213** are switched on when a voltage is being applied to the first plane **102** and are switched off when a voltage is being applied to the second plane **103**. Similarly, when a voltage is being applied to the second plane **103**, transistors **212** and **215** are switched on with transistors **211** and **213** being switched off. In the configuration shown in **FIG. 2**, with switch **221** receiving an input from buffer **222**, output transistors **211** and **213** are switched off with output transistors **212** and **215** being switched on. This is achieved by output pin CO being placed in a high condition and pin Cl being placed in a low condition. Similarly, pin C3 is placed in a low condition and pin C4 is placed in a high condition.

[0045] In the configuration shown, C3 is placed in a low condition, as previously described. The micro-controller **201** includes a pull-down transistor arranged to sink current from the base of transistor **212**, resulting in transistor **212** being switched on to saturation. Consequently, transistor **212** appears as having a very low resistance, thereby placing terminal **111** at the supply voltage of five volts. Resistor **231** (4K7) limits the flow of current out of the micro-controller **201**, thereby preventing burn-out of the micro-controller's output transistor.

[0046] Pin C4 is placed in a high state, resulting in transistor **215** being placed in a conducting condition. A serial resistor is not required given that the micro-controller **201** includes internal pull-up resistors, as distinct from a pull-up transistor, such that current flow is restricted. Thus, transistors **212** and **215** are both rendered conductive, resulting in terminal **111** being placed at the positive supply rail voltage and terminal **112** being placed at ground voltage. The capacitors shown in the circuit, such as capacitor **219**, limit the rate of transistor transitions thereby reducing rf transmissions from the sensor **101**.

[0047] With transistors **212** and **215** placed in their conductive condition, input signals are received from the first plane **102** in the form of a voltage applied to terminal **108**. For position detection, this voltage is measured directly and transistor **214** is placed in a non-conductive condition by output pin C2 being placed in a low condition. Under these conditions, the voltage from input terminal **108** is applied to analogue to digital converter **203** via buffer **222** and switch **221**.

[0048] In accordance with the present invention, a second electrical property is determined which, in this embodiment, represents the current flowing through the sensor in response to a mechanical interaction. The current measurement is made by placing transistor **214** in a conductive condition, by placing output pin C2 in a high condition. In this condition, current received at terminal **108** is supplied to transistor **214** via resistor **214**A, having a resistance of typically 5 k selectable so as to correspond to the characteristics of the sensor. A voltage is supplied to A to D converter **203** via buffer **222** and switch **221** but on this occasion the voltage represents a voltage drop, and hence a current, across resistor **214**A.

[0049] Thus, transistors **212** and **215** are placed in a conducting condition, transistor **214** is placed in a nonconducting condition, so as to measure voltage, and is then placed in a conducting condition so as to measure current. The roles of the transistors are then reversed, such that output transistors **211** and **213** are placed in a conducting condition, with transistors **212** and **215** being placed in a non-conducting condition (and switch **221** reversed) allowing a voltage to be measured by placing transistor **216** in a non-conducting condition, and then allowing a current to be measured by placing transistor **216** in a conducting condition.

[0050] The cycling of line conditions, in order to make the measurements identified previously, is controlled by a clock resident within micro-controller **201**. After each condition has been set up, a twelve bit number is received from the digital to analogue converter **203** and this number is retained within a respective register within micro-controller **201**. Thus, after completing a cycle of four measurements, four twelve bit values are stored within the micro-controller **201** for interrogation by the processing device **131**. Furthermore, the rate of cycling may be controlled in response to instructions received from the processing device **131**.

[0051] Operations performed by micro-controller **201** are detailed in **FIG. 3**. The micro-controller continually cycles between its four configuration states and each time a new input is produced, representing a current or a voltage in one of the two configurations, new output data is calculated on an on-going basis. Thus, output registers are updated such that the best data is made available if the micro-controller is interrupted by the external processor **131**.

[0052] The micro-controller **201** is fully interrupt driven in terms of receiving external interrupts for data interrogation along with internal interrupts in order to initiate a configuration cycle. The external interrupt has a higher priority such that external processor **131** is provided with information as soon as possible in response to making an interrupt request.

[0053] Internally interrupts for the micro-controller **201** are generated by its own internal timer and the procedure shown in **FIG. 3** is effectively held in a wait state until a next timer interrupt is received at step **301**. The wait state allows voltage levels on connections **107**, **108**, **111** and **112** to become stable and provides sufficient time for valid data to be received from the analogue to digital converter **203**.

[0054] At step **302**, an output is received from analogue to digital converter **203** and at step **303** calculations are performed with respect to the most current data received from the analogue to digital converter, so as to convert numerical values relating to voltages and currents into numerical values representing properties of the mechanical interaction. Thus, after performing calculations at step **303**, appropriate registers are updated at step **304** and it is these registers that are interrogated in response to an interrupt received from processing system **131**.

[0055] At step **305** next conditions for the output lines are set by appropriate logic levels being established for output pins CO to C6. After the next output condition has been selected, the processor enters a wait state at step **306**, allowing the electrical characteristics to settle, whereafter processing continues in response to the next timer interrupt.

[0056] Thus, it should be appreciated that on each iteration of the procedure shown in **FIG. 3**, one of the output conditions is selected at step **305**. Thus, it should be appre-